Record Maximum Transconductance of 3.45 mS/μm for III–V FETs

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***Abstract*— This letter presents a self-aligned InGaAs quantum-well MOSFET with a transconductance, $g_{m,max}$, of 3.45 mS/μm at V_{ds} = 0.5 V. This is a record value among III–V FETs of any kind, including MOSFETs and HEMTs, and represents an improvement of over 10% with respect to the previous record on planar devices. This result was achieved by redesigning the access regions that link the intrinsic device to the source and drain contacts so as to increase their electron concentration. This mitigates the nonlinear increase of the access resistance at high current. This is often referred to as source starvation and leads to the loss of transconductance under strong ON conditions.**

***Index Terms*— III–V FETs, quantum-well MOSFETs, transconductance, virtual source.**

I. Introduction

InAs-RICH InGaAs is a promising channel material for future high-performance low-power CMOS applications due to its superior electron transport properties [1]. There have recently been tremendous research efforts towards developing InGaAs MOSFET technology [2]. Various device integration schemes for planar devices have been demonstrated, including regrown SD [3]–[5], implanted SD [6], "nickelide" SD [7], [8], recessed-gate technology [9]–[11], and combinations of the above [12].

The self-aligned recessed-gate approach has arisen as one of the most promising technologies due to its process simplicity and high performance [9], [13]. Our fabrication technology can achieve precise control of critical transistor dimensions that include gate length, channel thickness, and access regions length and thickness [14]. The unprecedented channel geometry control that this technology affords makes this device structure an ideal vehicle to study device physics of relevance for future CMOS applications. In this regard, we have carried out studies on nanoscale Mo/n^+ InGaAs contacts [14], ballistic resistance [15], impact of channel thickness scaling on transport and short channel effects [16] and OFF-state leakage originating from the coupling of band-to-band tunneling (BTBT) and floating-body bipolar gain effects [17].

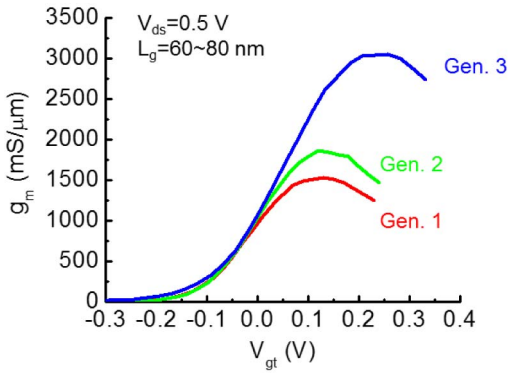

Fig. 1. Saturated g_m vs. gate overdrive, $V_{gt} = V_{gs} - V_t$, in high-performance self-aligned InGaAs QW-MOSFETs over three generations of device technology [9], [14], [19].

A key performance figure-of-merit for any transistor is its transconductance, g_m. At the present time, the highest g_m of planar InGaAs MOSFETs is 3.1 mS/μm obtained at V_{ds} = 0.5 V in self-aligned recessed gate QW-MOSFETs [14]. This value of transconductance matches that of the best InGaAs HEMTs to-date [18].

An analysis of g_m in high performance InGaAs QW-MOSFETs over several generations strongly suggests that g_m is limited by a high current effect. This is seen in Fig. 1 where g_m for different transistors with similar channel design and gate length is plotted as a function of gate overdrive [9], [14], [19]. While the low current g_m characteristics closely match among all devices, g_m diverges as the current level increases. What is different among these three device generations is the design of the access regions. Gen. 1 is fabricated by a wet etch process that provides poor control [19]. In consequence, the access region is devoid of an n^+ ledge. The resulting underlapped device has the lowest carrier concentration in the access region among the three designs. Gen. 2 ("long-ledge" in [9]) is covered by a thin n^+ cap that has been etched by digital etching. Gen. 3 has a thick n^+ cap and the highest access-region electron concentration among the three [14]. This analysis suggests that the carrier concentration, N_s, in the access regions is crucial to achieve high g_m.

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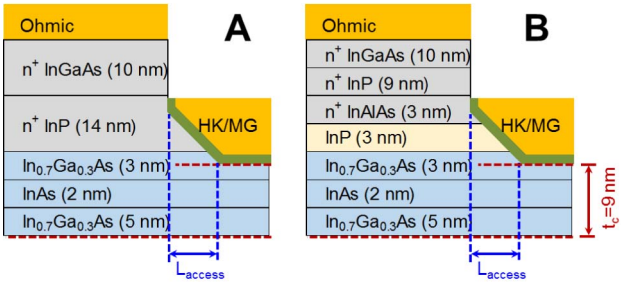

Fig. 2. Cross-sectional schematics for two simplified devices and the respective heterostructures, A and B (see text), used in this experiment with layer thickness in parenthesis. Layers labeled with n^+ are Si-doped with $N_D = 3 \times 10^{19} - 4 \times 10^{19}$ cm^{-3}, otherwise they are undoped. Intrinsic channel thickness is $t_c = 9$ nm.

With this insight, in this letter, we deliberately explore the role of N_s in the access region of InGaAs MOSFETs by fabricating otherwise identical transistors with two different access region designs. We observe a marked improvement in current capability and g_m in the devices with the highest N_s in their extrinsic region. In fact, this work has led to a new record transconductance value for planar InGaAs FETs of any kind of 3.45 mS/μm at $V_{ds} = 0.5$ V.

II. Key Technology Elements

Fig. 2 shows two heterostructure designs, labeled A and B, used in this work. They are identical except for the design of the n^+ cap. Design A features a thick and heavily doped n^+ InP layer directly on top of the channel while B features an undoped InP spacer between the n^+ cap and the channel. Design B is similar to our earlier devices. The elimination of the undoped InP spacer in design A results in a higher electron density in the InGaAs/InAs/InGaAs channel layer in the as-grown structure, as discussed below. An n^+ InP cap contact directly on InGaAs channel has been demonstrated in [11].

We have fabricated devices with various gate lengths and channel thicknesses using a process that closely follows that of [13] and [14]. For the devices reported in this letter, the intrinsic channel thickness is 9 nm (Fig. 2) which is the optimum thickness for ON-state performance in this channel structure [16]. The high$-\kappa$ gate dielectric is 2.5 nm HfO_2 with an estimated equivalent oxide thickness (EOT) of 0.5 nm. In both devices, we use the same tight access region design with $L_{access} = 15$ nm. Both samples A and B were processed at the same time.

The heart of our device fabrication process is the recessed-gate technology which uses dry etch and self-limiting digital etch (DE) to realize precise dimensional control over critical transistor dimensions. The tight self-aligned design that it affords is essential for high performance. For this reason, extensive dry etch including F-based oxide and metal RIE and Cl-based III-V cap RIE are used in our process. To ensure high surface quality after cap recess, careful optimization of the dry etch conditions was performed [13]. In our best results, we have been able to demonstrate a post-etch (RIE plus digital etch) exposed intrinsic InGaAs channel with surface roughness characterized by RMS = 0.2 nm. Long-channel ($L_g = 1$ μm) devices with a channel thickness $t_c = 3$ nm fabricated in sample A exhibit a subthreshold swing of 66.6 mV/dec at $V_{ds} = 10$ mV, matching the lowest S obtained in any planar InGaAs MOSFET [20].

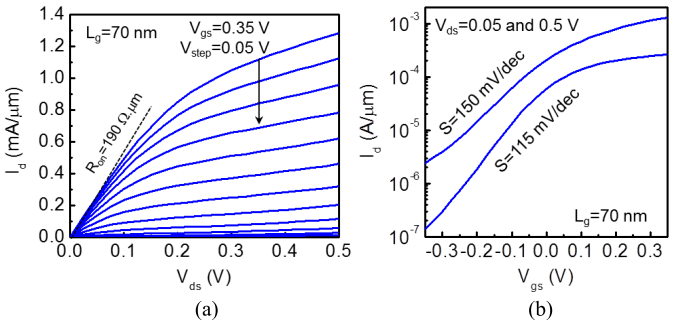

Fig. 3. (a) Output I_d-V_{ds} and (b) Transfer I_d-V_{gs} characteristics for InGaAs MOSFET of design A with $L_g = 70$ nm.

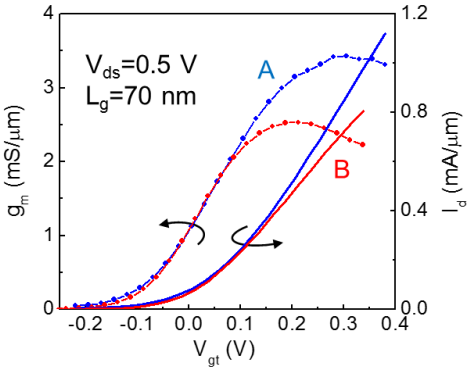

Fig. 4. Transconductance g_m versus V_{gt} and transfer characteristics I_d-V_{gt} of MOSFETs A and B with $L_g = 70$ nm.

III. The Record InGaAs MOSFET

The output characteristics of a design-A InGaAs MOSFET with $L_g = 70$ nm are shown in Fig. 3(a). The device exhibits an extremely low ON resistance of 190 $\Omega.\mu$m. Fig. 3(b) shows the transfer characteristics of the same device for $V_{ds} = 0.05$ and 0.5 V in semilog scale. The subthreshold swing is 150 mV/dec at $V_{ds} = 0.5$ V and 115 mV/dec at $V_{ds} = 50$ mV. The measure of drain-induced barrier lowering (DIBL) is 220 mV/V. The output conductance measured at the highest V_{gs} and V_{ds} in Fig. 3 is $g_d = 1.05$ mS/μm. The degradation of subthreshold swing at high V_{ds} and negative V_{gs} is the consequence of BTBT coupled with the floating-body effect [17]. In small gate length planar InGaAs MOSFETs, the current gain of the parasitic, floating-base, bipolar transistor increases rapidly as L_g is reduced and it multiplies the BTBT-generated hole current. No effort has been made in these device designs to mitigate this problem.

Fig. 4 shows g_m and I_d vs. gate overdrive ($V_{gt} = V_{gs} - V_t$) of devices with $L_g = 70$ nm of designs A and B. Design A device achieves a $g_{m,max} = 3.45$ mS/μm at $V_{ds} = 0.5$ V. This represents an 11% improvement over the previous records in planar InGaAs MOSFETs and HEMTs, both at 3.1 mS/μm [14], [18]. Peak transconductances at $V_{ds} = 0.5$ V vary from

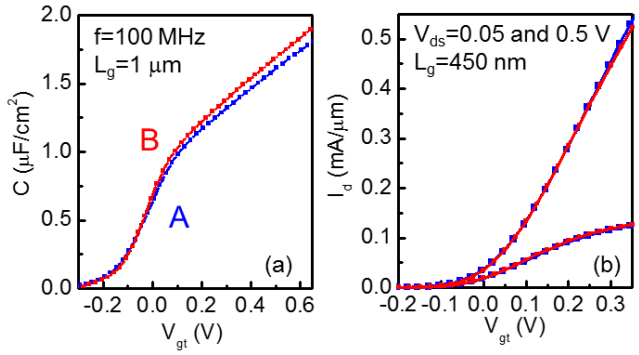

Fig. 5. (a) Gate capacitance and (b) Drain current versus gate overdrive V_{gt} for the long-channel A and B devices. C-V is measured with source and drain tied together at a frequency of 100 MHz. Gate overlap capacitance obtained at $V_{gt} = -0.3$ V is subtracted from the measured capacitance.

3.2 to 3.45 mS/μm across 6 identical devices of the same gate length on the same chip. Design B device shows $g_{m,max} = 2.55$ mS/μm at $V_{ds} = 0.5$ V. Peak transconductances at $V_{ds} = 0.5$ V vary from 2.4 to 2.55 mS/μm in this sample. It is interesting to note that the low-current g_m characteristics of these two devices match very closely while they diverge at high values of I_d. This is consistent with the data in Fig. 1. For the transfer and output sweeps, V_{gt} were kept below 0.4 V to avoid any positive gate bias stress on the device.[1] For this gate voltage range, threshold voltage hysteresis (ΔV_t) of less than 15 mV and peak g_m difference of less than 3% between up- and down-ward gate sweeps are observed.

The fact that these two device designs have closely matched intrinsic channels is further confirmed by split-C-V (Fig. 5a) and transfer I_d-V_{gs} characteristics (Fig. 5b) that are measured in devices with L_g between 450 nm and 1 μm. The long-channel characteristics in samples A and B show very little difference and suggest that the difference between the g_m data in Fig. 4 is a high-current effect.

To further support this hypothesis, we have extracted the external series resistance R_{EXT} from R_{on} versus effective gate length (not shown) for both sets of devices [15]. The values are 75 and 125 $\Omega.\mu$m for samples A and B, respectively. In the short-channel devices (Fig. 4), this difference is not sufficient to explain the different peak g_m values of transistors A and B. That is, obtaining intrinsic g_m using the extracted constant R_{EXT} yields a peak g_{mi} for A and B of 3.9 mS/μm and 3.0 mS/μm respectively. Including the effect of output conductance [21], the peak g_{mi} for A and B are 4.4 mS/μm and 3.6 mS/μm, respectively.

IV. Limits to Maximum Transconductance

The loss of g_m at high current levels in HEMTs has been attributed to velocity saturation in the source-side access region [22]. In our devices, the access regions are very short ($L_{access} = 15$ nm) and operate under ballistic transport. Hence, the g_m loss cannot be attributed to velocity saturation. An alternative explanation is source starvation, as predicted in [23] and discussed below.

The behavior of short-channel MOSFETs operating in saturation can be described by the so-called top-of-the-barrier or virtual-source (VS) charge-control-injection model [24]. In this model the device current is determined by the product of the sheet charge concentration at VS, Q_{VS}, and the average carrier injection velocity at the same location, v_{inj}. In very short devices and in particular in III-V FETs, v_{inj} is very close to the unidirectional thermal velocity, v_T. The theoretical limit for the maximum current that a transistor can drive in saturation when it operates in the full ballistic limit is $Q_{VS} \cdot v_T$.

At moderate gate overdrive, the VS is located at the source-edge of the channel under the gate. Under these conditions, the source access region, similar to the n^+-doped source in a Si MOSFET, is able to supply the VS with electrons while remaining at near equilibrium conditions. Within this view, the Q_{VS} versus V_{gs} relationship obtained by either integrating the long-channel capacitance in split-C-V measurements or solving the equilibrium charge-control equations without invoking any transport models, is a good representation of Q_{VS} in a near-ballistic short-channel MOSFET.

At high current, electrons in the source access region with wavevector **k** aligned along the transport direction can be depleted due to insufficient carrier density or momentum relaxation rate [23]. When this happens, the above assumption of near-equilibrium source access region fails. It is known that the density of states in high-mobility III-V materials is low and the mean scattering time is long. This implies that the distribution of carriers in the source access region can be driven out of equilibrium relatively easily. In this instance, in devices where there is no abrupt metallurgical junction between the highly doped source and channel, such as is the case here, the VS location would move beyond the edge of the gate into the source access region at high I_d. In other words, as I_d increases, the "channel" starts including an increasing portion of the access region. While the carrier velocity in this region is still close to v_T, the gate control over the charge at the new VS is diminished because of the reduced capacitive coupling (increased distance) with the gate. Since g_m is proportional to the gate-VS coupling capacitance, this phenomenon brings g_m down. To fully quantify this effect requires 2D Poisson-Schrödinger simulations coupled with a ballistic transport model which is beyond the scope of this work.

Within this source starvation concept, increasing the carrier concentration in the access regions of the device mitigates the problem, that is, it pushes its onset to a higher current level. That is what device design A accomplishes over device design B. Using Poisson-Schrodinger simulations and under the simplistic assumption of a passivated surface and $V_{gs} = 0$, the sheet electron concentration in the channel in the middle of the access region in device A is estimated to be 4.9×10^{12} cm^{-2} and in device B 1.0×10^{12} cm^{-2}. Consistent with this, a $g_{m,max}$ of 3.75 mS/μm is observed in our A devices at $V_{ds} = 0.7$ V, indicating that the source access region can support very high drain current. However, at this bias, strong

[1] It should be noted that the higher $g_{m,max}$ reported for devices of design B in [14] were partly the result of having measured the devices over a broad range of V_{gt}. We subsequently realized that this resulted in a temporary boost of $g_{m,max}$, through a mechanism that is currently under investigation. Limiting V_{gt} to below 0.4 V in this study has avoided any instability that could confuse the analysis.

impact ionization and floating body effect were observed. Therefore, the behavior of the device is out of its normal range of operation and hence is not discussed in this letter.

V. Conclusion

This letter presents a self-aligned planar InGaAs quantum-well MOSFET with maximum transconductance, $g_{m,max}$, of 3.45 mS/μm at $V_{ds} = 0.5$ V. This is a record value among planar III-V FETs of any kind, including MOSFETs and HEMTs. This result has been obtained by redesigning the access regions to increase their carrier concentration. These results are consistent with an important limiting factor to attain high current and high transconductance in III-V FETs, namely source starvation and associated migration of the virtual source point into the access region where gate control is diminished.

References

[1] J. A. del Alamo, "Nanometre-scale electronics with III–V compound semiconductors," *Nature*, vol. 479, no. 7373, pp. 317–323, Nov. 2011, doi: 10.1038/nature10677.

[2] H. Riel, L.-E. Wernersson, M. Hong, and J. A. del Alamo, "III–V compound semiconductor transistors—From planar to nanowire structures," *MRS Bull.*, vol. 39, no. 8, pp. 668–677, Aug. 2014, doi: http://dx.doi.org/10.1557/mrs.2014.137.

[3] M. Egard, L. Ohlsson, B. M. Borg, F. Lenrick, R. Wallenberg, L.-E. Wernersson, and E. Lind, "High transconductance self-aligned gate-last surface channel $In_{0.53}Ga_{0.47}As$ MOSFET," in *IEDM Tech. Dig.*, Dec. 2011, pp. 13.2.1–13.2.4, doi: 10.1109/IEDM.2011.6131544.

[4] S. Lee, C.-Y. Huang, A. D. Carter, D. C. Elias, J. J. M. Law, V. Chobpattana, S. Kramer, B. J. Thibeault, W. Mitchell, S. Stemmer, A. C. Gossard, and M. J. W. Rodwell, "Record extrinsic transconductance (2.45 mS/μm at VDS = 0.5 V) InAs/$In_{0.53}Ga_{0.47}As$ channel MOSFETs using MOCVD source-drain regrowth," in *Proc. VLSI Technol.*, Jun. 2013, pp. T246–T247.

[5] X. Zhou, Q. Li, C. W. Tang, and K. M. Lau, "30 nm enhancement-mode $In_{0.53}Ga_{0.47}As$ MOSFETs on Si substrates grown by MOCVD exhibiting high transconductance and low on-resistance," in *IEDM Tech. Dig.*, Dec. 2012, pp. 32.5.1–32.5.4, doi: 10.1109/IEDM.2012.6479153.

[6] J. Lin, S. Lee, H.-J. Oh, W. Yang, G. Q. Lo, D. L. Kwong, and D. Z. Chi, "Plasma PH3-passivated high mobility inversion InGaAs MOSFET fabricated with self-aligned gate-first process and HfO_2/TaN gate stack," in *IEDM Tech. Dig.*, Dec. 2008, pp. 1–4, doi: 10.1109/IEDM.2008.4796705.

[7] S. Kim, M. Yokoyama, R. Nakane, O. Ichikawa, T. Osada, M. Hata, M. Takenaka, and S. Takagi, "High performance tri-gate extremely thin-body InAs-on-insulator MOSFETs with high short channel effect immunity and *V*th tunability," in *IEDM Tech. Dig.*, 2013, pp. 16.4.1–16.4.4, doi: 10.1109/IEDM.2013.6724642.

[8] S. W. Chang, X. Li, R. Oxland, S. W. Wang, C. H. Wang, R. Contreras-Guerrero, K. K. Bhuwalka, G. Doornbos, T. Vasen, M. C. Holland, G. Vellianitis, M. J. H. van Dal, B. Duriez, M. Edirisooriya, J. S. Rojas-Ramirez, P. Ramvall, S. Thoms, U. Peralagu, C. H. Hsieh, Y. S. Chang, K. M. Yin, E. Lind, L.-E. Wernersson, R. Droopad, I. Thayne, M. Passlack, and C. H. Diaz, "InAs N-MOSFETs with record performance of Ion = 600 μA/μm at Ioff = 100 nA/μm (Vd = 0.5 V)," in *IEDM Tech. Dig.*, Dec. 2013, pp. 16.1.1–16.1.4, doi: 10.1109/IEDM.2013.6724639.

[9] J. Lin, X. Zhao, T. Yu, D. A. Antoniadis, and J. A. del Alamo, "A new self-aligned quantum-well MOSFET architecture fabricated by a scalable tight-pitch process," in *IEDM Tech. Dig.*, vol. 2013, pp. 16.2.1–16.2.4, doi: 10.1109/IEDM.2013.6724640.

[10] T.-W. Kim, D. Kim, D.-H. Koh, R. J. W. Hill, R. T. P. Lee, M. H. Wong, T. Cunningham, J. A. del Alamo, S. K. Banerjee, S. Oktyabrsky, A. Greene, Y. Ohsawa, Y. Trickett, G. Nakamura, Q. Li, K. M. Lau, C. Hobbs, P. D. Kirsch, and R. Jammy, "ETB-QW InAs MOSFET with scaled body for improved electrostatics," in *IEDM Tech. Dig.*, Dec. 2012, pp. 32.3.1–32.3.4, doi: 10.1109/IEDM.2012.6479151.

[11] Y. Yonai, T. Kanazawa, S. Ikeda, and Y. Miyamoto, "High drain current (>2A/mm) InGaAs channel MOSFET at VD = 0.5 V with shrinkage of channel length by InP anisotropic etching," in *IEDM Tech. Dig.*, Dec. 2011, pp. 13.3.1–13.3.4, doi: 10.1109/IEDM.2011.6131545.

[12] A. Majumdar, Y. Sun, C.-W. Cheng, Y.-H. Kim, U. Rana, R. M. Martin, R. L. Bruce, K.-T. Shiu, Y. Zhu, D. B. Farmer, M. Hopstaken, E. A. Joseph, J. P. de Souza, M. M. Frank, S.-L. Cheng, M. Kobayashi, E. A. Duch, D. K. Sadana, D.-G. Park, and E. Leobandung, "CMOS-Compatible Self-Aligned $In_{0.53}Ga_{0.47}As$ MOSFETs with gate lengths down to 30 nm," *IEEE Trans. Electron Devices*, vol. 61, no. 10, pp. 3399–3404, Oct. 2014, doi: 10.1109/TED.2014.2335747.

[13] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "A CMOS-compatible fabrication process for scaled self-aligned InGaAs MOSFETs," in *Proc. CS MANTECH*, 2015, p. 12.2.

[14] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Novel intrinsic and extrinsic engineering for high-performance high-density self-aligned InGaAs MOSFETs: Precise channel thickness control and sub-40-nm metal contacts," in *IEDM Tech. Dig.*, Dec. 2014, pp. 25.1.1–25.1.4, doi: 10.1109/IEDM.2014.7047104.

[15] J. Lin, Y. Wu, J. del Alamo, and D. A. Antoniadis, "Analysis of resistance and mobility in InGaAs quantum-well MOSFETs from ballistic to diffusive regimes," *IEEE Trans. Electron Devices*, 2016, doi: 10.1109/TED.2016.2532604.

[16] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Impact of intrinsic channel scaling on InGaAs quantum-well MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 11, pp. 3470–3476, Nov. 2015, doi: 10.1109/TED.2015.2444835.

[17] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Off-state leakage induced by band-to-band tunneling and floating-body bipolar effect in InGaAs quantum-well MOSFETs," *IEEE Electron Device Lett.*, vol. 35, no. 12, pp. 1203–1205, Dec. 2014, doi: 10.1109/LED.2014.2361528.

[18] X. Mei, W. Yoshida, M. Lange, J. Lee, J. Zhou, P.-H. Liu, K. Leong, A. Zamora, J. Padilla, S. Sarkozy, R. Lai, and W. R. Deal, "First demonstration of amplification at 1 THz using 25-nm InP high electron mobility transistor process," *IEEE Electron Device Lett.*, vol. 36, no. 4, pp. 327–329, Apr. 2015, doi: 10.1109/LED.2015.2407193.

[19] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30 nm InAs quantum-well MOSFETs with self-aligned metal contacts and sub-1 nm EOT HfO_2 insulator," in *IEDM Tech. Dig.*, Dec. 2012, pp. 32.1.1–32.1.4, doi: 10.1109/IEDM.2012.6479149.

[20] M. Radosavljevic, G. Dewey, D. Basu, J. Boardman, B. Chu-Kung, J. M. Fastenau, S. Kabehie, J. Kavalieros, V. Le, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, H. W. Then, and R. Chau, "Electrostatics improvement in 3-D tri-gate over ultra-thin body planar InGaAs quantum well field effect transistors with high-*K* gate dielectric and scaled gate-to-drain/gate-to-source separation," in *IEDM Tech. Dig.*, Dec. 2011, pp. 33.1.1–33.1.4, doi: 10.1109/IEDM.2011.6131661.

[21] S. Y. Chou and D. A. Antoniadis, "Relationship between measured and intrinsic transconductances of FET's," *IEEE Trans. Electron Devices*, vol. 34, no. 2, pp. 448–450, Feb. 1987, doi: 10.1109/T-ED.1987.22942.

[22] D. R. Greenberg and J. A. del Alamo, "Velocity saturation in the extrinsic device: A fundamental limit in HFET's," *IEEE Trans. Electron Devices*, vol. 41, no. 8, pp. 1334–1339, Aug. 1994, doi: 10.1109/16.297726.

[23] M. V. Fischetti, L. Wang, B. Yu, C. Sachs, P. M. Asbeck, Y. Taur, and M. Rodwell, "Simulation of electron transport in high-mobility MOSFETs: Density of states bottleneck and source starvation," in *IEDM Tech. Dig.*, Dec. 2007, pp. 109–112, doi: 10.1109/IEDM.2007.4418876.

[24] Y. Liu, M. Luisier, A. Majumdar, D. A. Antoniadis, and M. S. Lundstrom, "On the interpretation of ballistic injection velocity in deeply scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. 59, no. 4, pp. 994–1001, Apr. 2012, doi: 10.1109/TED.2012.2183599.